

EAST - [10733043b.wsp:1]

File View Edit Tools Window Help

Drafts Pending Active L1: (624) 257/302.CCLS L2: (172) 1 and (trench near capacitor and source and gate and substrate) L3: (12) 2 and (gate near substrate) Failed Saved Favorites Tagged (1) UDC Queue Trash

DBs: US-PGPUB-USPAT-EPO-JFO

Default operator: OR

257/302.CCLS

BRD form ISAR form Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
260	<input type="checkbox"/>	<input type="checkbox"/>	US 6380575 B1	20020430	7	DRAM trench cell	257/296	257/301; 257/302; 257/307	2
281	<input type="checkbox"/>	<input type="checkbox"/>	US 6376873 B1	20020423	43	Vertical DRAM cell with robust gate-to-storage node isolation	257/301	257/302; 257/303; 257/304	2
282	<input type="checkbox"/>	<input type="checkbox"/>	US 6376324 B1	20020423	12	Collar process for reduced deep trench edge bias	438/386	257/301; 257/302; 257/303	2
283	<input type="checkbox"/>	<input type="checkbox"/>	US 6373091 B1	20020416	7	Vertical DRAM cell with TFT over trench capacitor	257/306	117/8; 257/11; 257/301	2
284	<input type="checkbox"/>	<input type="checkbox"/>	US 6373086 B1	20020416	19	Notched collar isolation for suppression of vertical parasitic MOSFET and the method of preparing the same	257/301	257/302; 257/E21.653; 257/E29.346	2
285	<input type="checkbox"/>	<input type="checkbox"/>	US 6373065 B1	20020416	24	Semiconductor memory cell having two epitaxial layers and its manufacturing method	257/301	257/302; 257/E27.093; 257/E29.346	2
286	<input type="checkbox"/>	<input type="checkbox"/>	US 6365452 B1	20020402	27	DRAM cell having a vertical transistor and a capacitor formed on the sidewalls of a trench	438/241	257/301; 257/302; 257/E21.653	2
287	<input type="checkbox"/>	<input type="checkbox"/>	US 6355974 B1	20020312	8	Method to prevent the formation of a thinner portion of insulating layer at the junction between the sidewalls and the bottom insulator	257/622	257/302; 257/328; 257/333	2
288	<input type="checkbox"/>	<input type="checkbox"/>	US 6344673 B1	20020205	23	Multilayered quantum conducting barrier structures	257/301	257/302; 257/E21.653; 257/E29.339	2
289	<input type="checkbox"/>	<input type="checkbox"/>	US 6339241 B1	20020115	39	Structure and process for 6F2 trench capacitor	257/301	257/296; 257/302; 257/303	2
290	<input type="checkbox"/>	<input type="checkbox"/>	US 6339239 B1	20020115	9	DRAM cell layout for node capacitance enhancement	257/296	257/301; 257/302; 257/E27.067	2

File Drafts HTML

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